

# Carbon nanotubes for interconnects in VLSI integrated circuits

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The paper reviews the requirements for carbon nanotubes to be used as interconnects in VLSI integrated circuits. It describes the production by chemical vapour deposition of high

density arrays of nanotubes suitable for use as interconnects, and describes their characterisation by Raman and transmission electron microscopy.

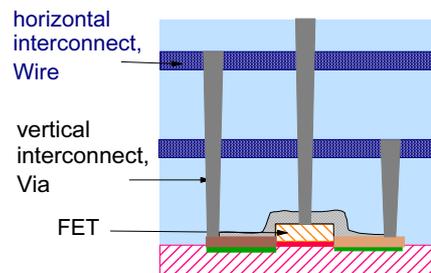
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**1 Introduction** The continued scaling of semiconductor devices in VLSI integrated circuits means that the current density carried by the interconnects which connect the transistors together (Fig. 1) will soon exceed the maximum the maximum allowed by Cu of  $\sim 6 \cdot 10^6$  A.cm<sup>-2</sup> before it fails due to electromigration. This is expected to occur at the 22 nm node (Fig. 2). Only carbon nanotubes have a higher current carrying capacity, and so they have been proposed as alternatives, being able to carry  $\sim 10^9$  Acm<sup>-2</sup> before failure [1-4]. As interconnects merely carry current, they are viewed as much simpler than carbon nanotube transistors, and might be expected to be one of the first implementations of nanotubes into electronics [5, 6]. Here, we consider the requirements for carbon nanotubes to be used as interconnects and note that they are actually quite demanding.

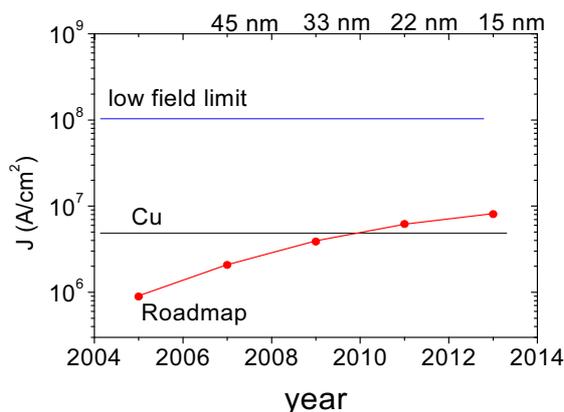
Carbon nanotubes have a high current carrying capacity and also have ballistic transport over short distances [1, 2]. However, being one-dimensional their conductivity is limited by one quantum of conductance  $G_0$  per band or ‘channel’,  $G_0 = 2e^2/h$ . This quantum conductance appears as a series resistance in the expression for their resistance as a function of length,

$$R = R_q + r L .$$

A nanotube interconnect must not only carry a high current, it should also have a lower resistance than the Cu unit that it replaces. As  $R_q = 12.6$  k $\Omega$  per channel, and there are two channels per wall of nanotube, the only way to lower the resistance is to have many conducting channels in parallel. This means either multi-walled nanotubes (MWNTs) in which all walls carry current, or a very high density of single walled nanotubes (SWNTs). Unless they are properly contacted, MWNTs tend to carry current mainly in their outer walls, but recently there is increased effort in making better contact to inner walls and forcing them to carry current. Nevertheless, we first consider the case of many parallel SWNTs.



(1) **Figure 1** Schematic cross-section of horizontal and vertical interconnects in an integrated circuit.



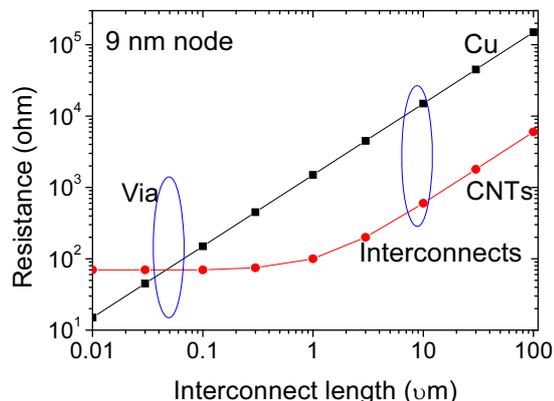
**Figure 2** Current density requirements vs Roadmap node, compared to the limiting current density of Cu.

Figure 3 compares the resistance of Cu and CNT interconnects of various lengths, using the resistance per unit length,  $r$ , of a SWNT which was extracted from data of McEuen et al. [7]. Note that nanotubes have two conduction regimes, low or high voltage [7, 8]; there is a large increase in resistance if the voltage exceeds the energy of the optic phonon of  $\sim 0.16$  V. Interconnects are designed to drop little voltage, so they will operate in the low voltage, low resistance regime.

Figure 3 shows that for a SWNT density of  $10^{14}$   $\text{cm}^{-2}$ , it is quite difficult to match the resistance of a Cu vertical interconnect (Via) of length 100 nm, while the major gain in using CNTs interconnect comes for longer, horizontal interconnects of typical length 10  $\mu\text{m}$ . There are two striking conclusions; first the desired SWNT density for Vias is huge, ideally  $10^{14}$   $\text{cm}^{-2}$ , on the theoretical limit. Second, vertical Vias are often perceived as the easier to implement because it is easier to grow CNTs vertically out of holes, whereas it is much more difficult to grow nanotubes horizontally. Figure 1 shows that the gain is most for horizontal interconnects.

The present status of work on Vias is that Kreupl et al. [5, 6] of Infineon did the early work on showing nanotube growth out of holes for Vias, but now the present leader is Awano et al. [9-11] of Fujitsu. They have achieved a MWNT density of over  $10^{11}$   $\text{cm}^{-2}$ , and are also working on the contacting problem.

**2 Growth for interconnects** Now consider if the manufacturing process for CNT interconnects should be ‘pick and place’ or grow in place. Electron beam lithography has a much higher resolution than optical lithography but it is not used for practical manufacturing because it is a serial process, which is orders of magnitude too slow. On the other hand, a parallel process like optical lithography prints the image of all 1 billion transistors at the same time. In the same way, CNT interconnects must use a parallel process like chemical vapour deposition (CVD), whereas serial pick and place is too slow to be of use.



**Figure 3** Low-field resistance of Cu and nanotube interconnects compared, as a function of their length.

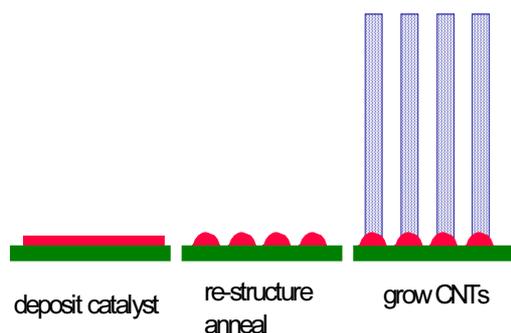
Interconnects are in the ‘back end of line’ (BEOL) process of integrated circuits, where the temperature cannot exceed 400 °C otherwise there is damage to the inter-layer dielectric, a low density form of  $\text{SiO}_x(\text{CH})_y$ .

There are thus five key issues for making CNT interconnects to consider;

- Density
- Growth temperature
- Fraction of metallic nanotubes
- Growth on metal surfaces
- Nanotube crystallinity and conductivity.

The highest density of nanotubes is found in vertically aligned arrays, mats or forests. Various groups have been able to grow vertical arrays of MWNTs and then SWNTs [12-16]. Most cases involve the growth using a catalyst of Fe on a support of  $\text{Al}_2\text{O}_3$ . The vertical alignment found in mats arises from their high density. Note that we are not particularly interested in the height of mats in our application, only the density. The highest density comes from an effort to optimise the combination of catalyst and support, their preparation conditions and growth conditions.

The temperature limits on nanotube growth need special consideration. The growth process consists of two stages; first the thin film deposited onto the support is annealed and converted into a series of catalyst nanoparticles, as in Fig. 4. Then the catalyst nucleates and grows its nanotube. In CVD, each catalyst particle forms one nanotube, of a similar diameter to itself. The restructuring of the catalyst into nano-particles occurs by creep, is thermally activated, and in fact is the rate-limiting step to nanotube growth. This stage should be carried out in a specially chosen atmosphere such as  $\text{NH}_3$ , without the hydrocarbon gas being present [17]. After this, the hydrocarbon growth gas is turned on, and nanotube growth is carried out. Using this method, Cantoro et al. [18] were able to lower the growth temperature of SWNTs by purely thermal CVD to about 400 °C. The whole process of catalyst re-structuring and nanotube growth has been observed by in-situ time-resolved TEM [19].

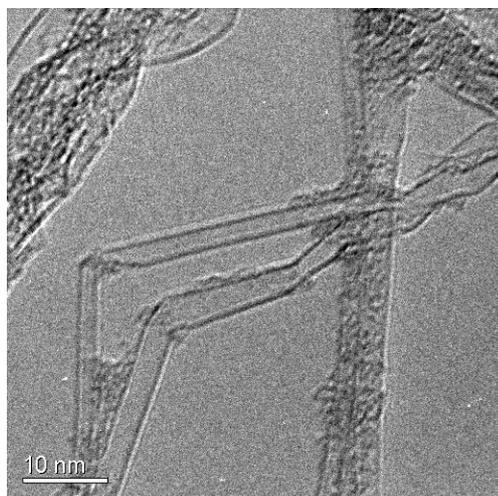


**Figure 4** Schematic of the catalyst activation and growth process for carbon nanotubes.

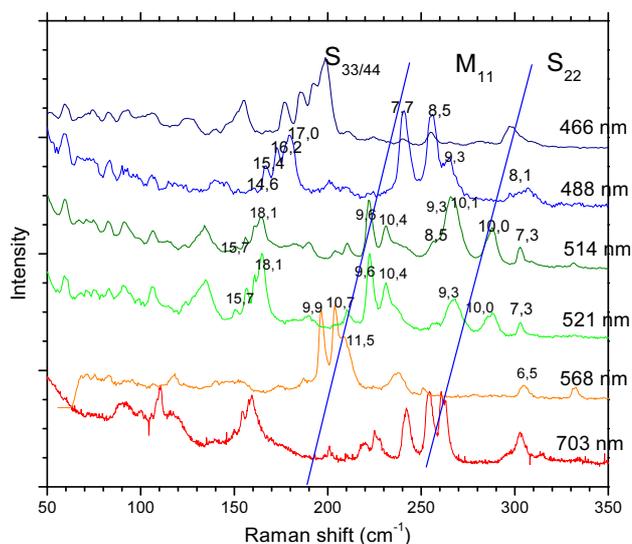
We grew the nanotubes using a catalyst of 0.5 to 1 nm of sputtered Fe on 5 nm of  $\text{Al}_2\text{O}_3$  formed by atmospheric oxidation of Al. The nanotubes were grown in a remote microwave PECVD reactor from an acetylene hydrogen gas mixture at 10 mbar pressure and a temperature of 600 °C [20].

**3 Characterization** Figure 5 shows transmission electron microscope (TEM) images of the resulting nanotubes. The TEM is a JEOL4000HR operated at 80 kV to reduce sample damage. The nanotubes are seen to be mainly large diameter SWNTs.

The area density of SWNTs grown in similar conditions by Zhong et al. [21] was  $\sim 10^{13} \text{ cm}^{-2}$ . Hata et al. [22] found that nanotubes grown from a similar catalyst were large walled SWNTs, becoming double walled NTs for larger catalyst sizes. They found a density of about  $5.2 \times 10^{11} \text{ cm}^{-2}$ . Thus, it appears that Fe on  $\text{Al}_2\text{O}_3$  tends to produce high densities of SWNTs but often of larger diameter tubes. Increasing the density will require catalyst optimisation to produce smaller diameter tubes. At present, our growth temperature is above 400 °C, but we expect to be able to lower this, without losing this density.



**Figure 5** TEM image of carbon nanotube mat.

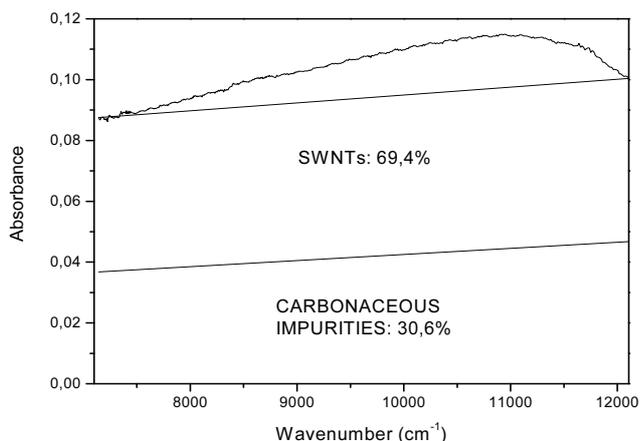


**Figure 6** Radial breathing mode sector of the Raman spectra at different excitation energies, plus the peak assignments. Central peaks are due to metallic tubes, those on left and right are due to semiconducting tubes.

The combination of Fe on  $\text{Al}_2\text{O}_3$  is unusual in producing the high density mats. This occurs because  $\text{Al}_2\text{O}_3$  promotes the de-wetting of Fe into nano-particles, but it also inhibits surface diffusion of Fe, so it inhibits the agglomeration of these nano-particles into larger droplets during growth [23].

The structure of SWNTs is defined by their chiral indices, which define whether a tube is metallic or semiconducting. CVD results in nanotubes with a distribution of chiralities. Various workers have lowered the growth temperature in CVD. This can lead to a narrowing of the chirality distribution [12]. Similarly, Dai [24] found that low temperature remote CVD formed 9 times as many semiconducting tubes as metallic, well above the 2:1 ratio in a random distribution. Obviously, interconnects require metallic tubes, so we must check on this. The usual means to measure the chirality is photoluminescence (PL) spectroscopy [25]. However, PL does not see metallic tubes, so instead we use resonant Raman spectroscopy [26, 27], which sees both types. However, variation of matrix elements means that the spectral intensities do not reflect the actual type distribution.

Figure 6 shows the radial breathing mode (RBM) part of the Raman spectrum of our samples measured at various wavelengths. The RBM wavenumber varies inversely with nanotube diameter. A Raman signal is seen when the excitation photon energy matches the transition energy of the nanotube. This varies roughly inversely with the nanotube diameter, but in a characteristic way with the chiral indices, as seen in a Kataura plot. A semi-empirical third-neighbour tight binding plot of Popov et al. [28] reproduces most of this energy distribution, including the exciton binding effects empirically. This allows us to index each of the peaks in the observed Raman spectra, as shown in Fig 6.



**Figure 7** Infra-red absorption spectra of carbon nanotube mats, for purity evaluation purposes.

The importance of this indexing is that it confirms that the sample contains a wide range of chiralities and diameters. It also contains many metallic chiralities. Thus, it is suitable for interconnects. A similar broad chirality distribution was found for Hata's 'super-growth' mats [29].

The purity of SWNTs samples is defined in terms of metallic impurities (catalyst) and graphitic or amorphous carbon impurities. The high efficiency of Fe/Al<sub>2</sub>O<sub>3</sub> catalyst and 'super growth' means that there the metal content is very low, of order 10 ppm. The amorphous carbon content was measured by infra-red absorption, using the method of Itkis et al. [30]. The SWNT content is found from the ratio of the S<sub>22</sub> peak heights, compared to the graphitic background. However, this method works best for a narrow chirality distribution, where the SWNTs introduce a few sharp peaks. It is less useful for a wide chirality distribution, where there will be numerous peaks, which are then less easy to distinguish from the background. With these caveats, we estimated a purity of 70%, as in Fig. 7. Note that the problem is that sidewall deposition of amorphous carbon can occur, if growth is continued for too long, or if the balance of etching gases is not correctly chosen.

Finally, interconnects must carry current, so they must be grown on metallic substrates. Al<sub>2</sub>O<sub>3</sub> is an insulator, so that it is not ultimately viable as a catalyst support for this application. Hence, with an understanding of many of the guiding principles, we must search for a different catalyst-support combination, which gives similar properties but is metallic. This could require the use of catalysts such as CoMoCAT [15], or the cluster deposition of Ni, Co or Fe catalyst on a Ta metal layer, as used by Fujitsu [31].

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